FIG. 1

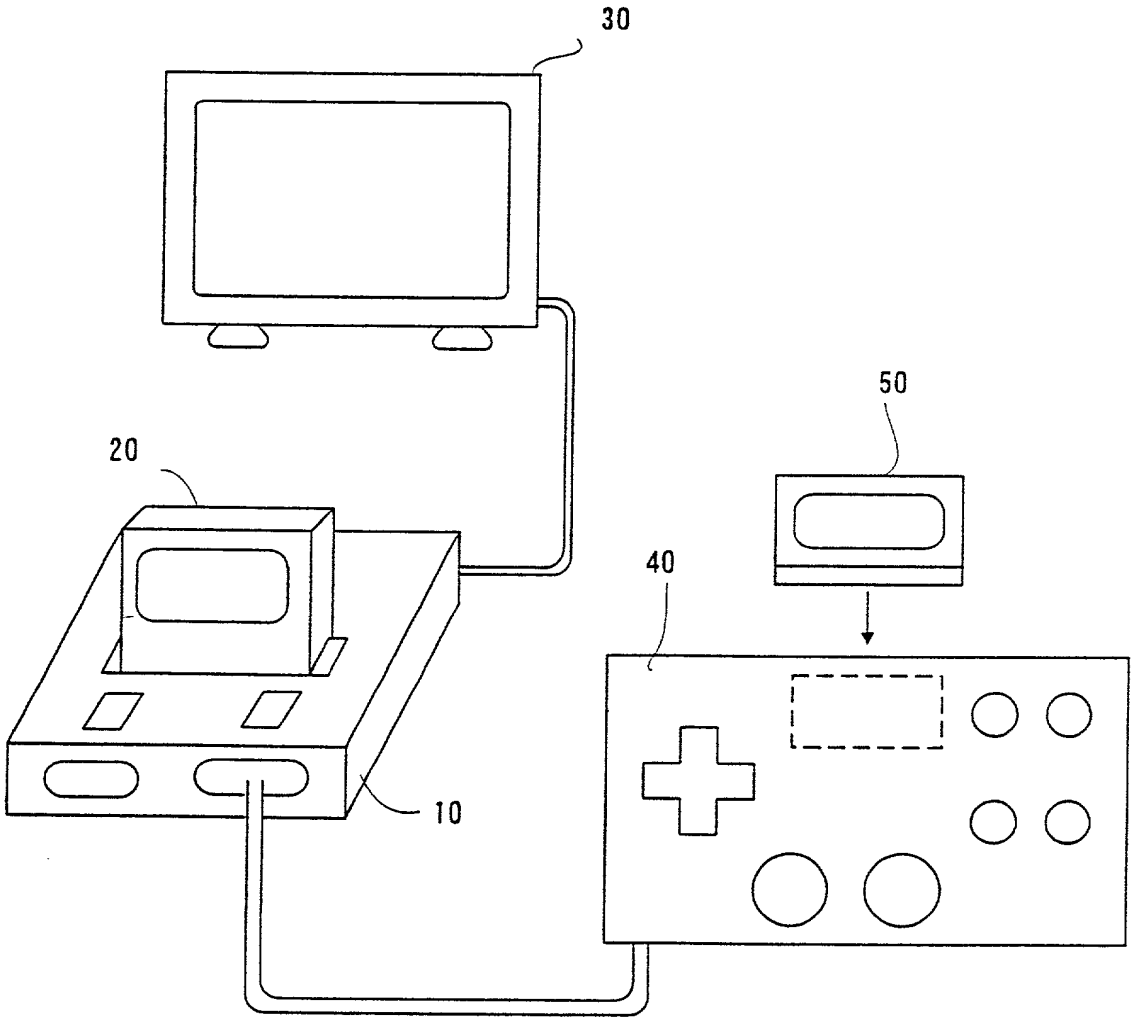


FIG. 2

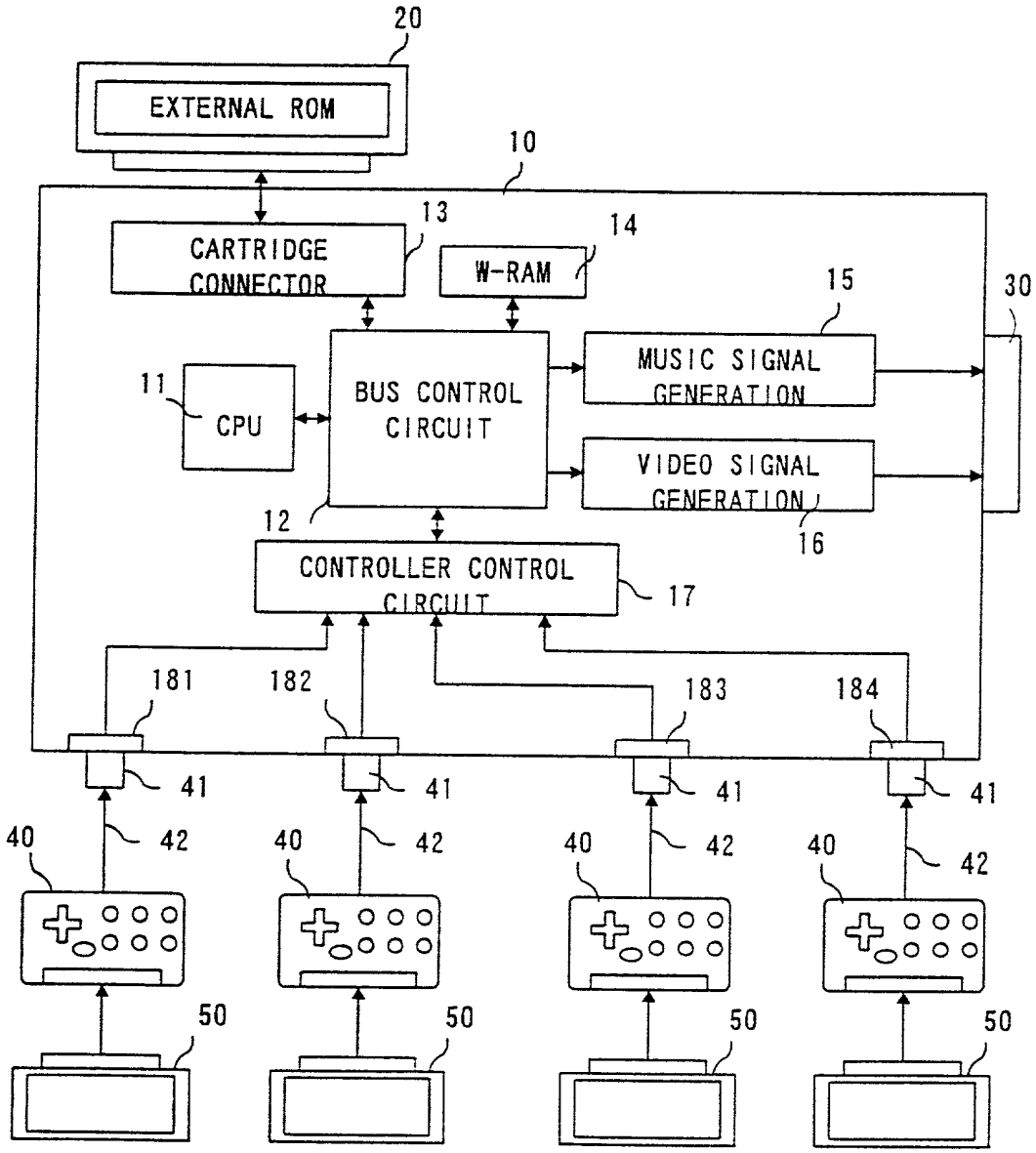

20
EXTERNAL ROM
10
CARTRIDGE CONNECTOR
13
W-RAM
14
15
30
MUSIC SIGNAL GENERATION
11
CPU
BUS CONTROL CIRCUIT
VIDEO SIGNAL GENERATION
16
12
CONTROLLER CONTROL CIRCUIT
17
181
182
183
184
41
42
40
50

FIG. 3

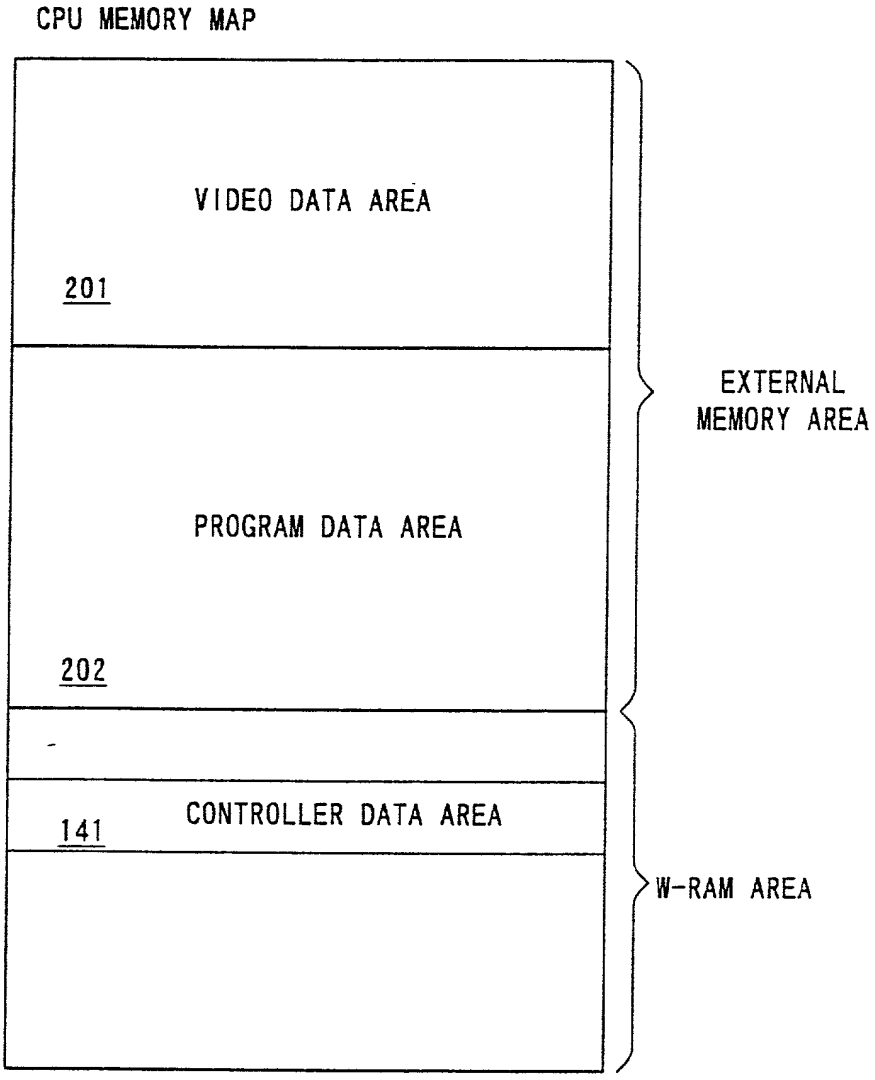

CPU MEMORY MAP
VIDEO DATA AREA
201
PROGRAM DATA AREA
202
CONTROLLER DATA AREA
141
EXTERNAL MEMORY AREA
W-RAM AREA

FIG. 4

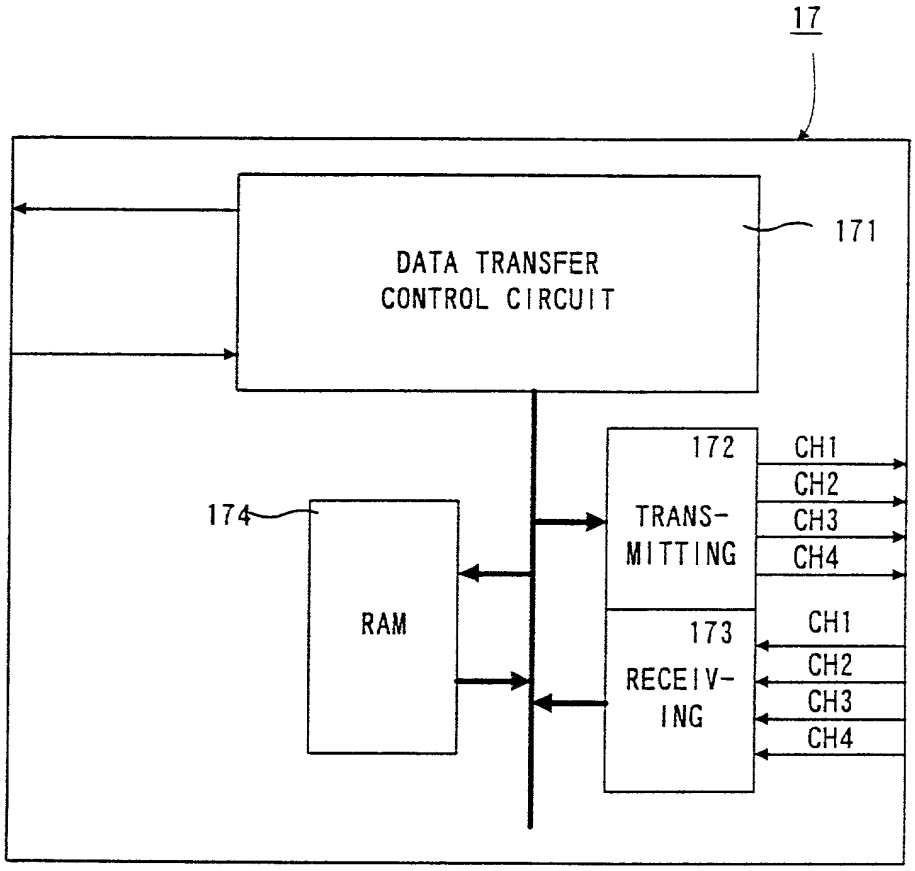
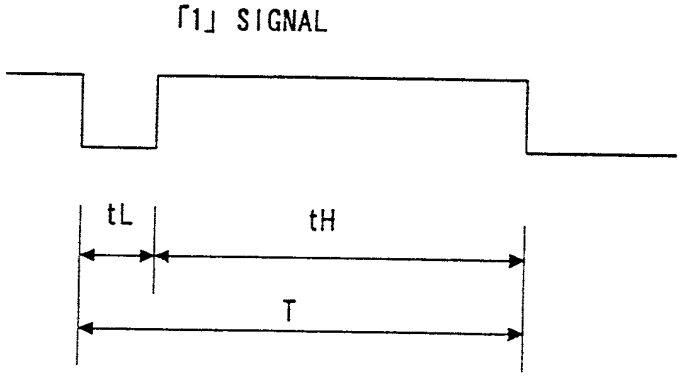

17
171
DATA TRANSFER
CONTROL CIRCUIT
172
TRANS-
MITTING
CH1
CH2
CH3
CH4
174
RAM
173
RECEIV-
ING
CH1
CH2
CH3
CH4

FIG. 5



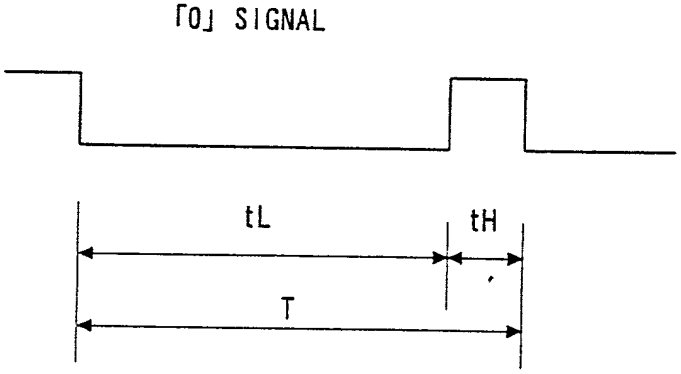


FIG. 6

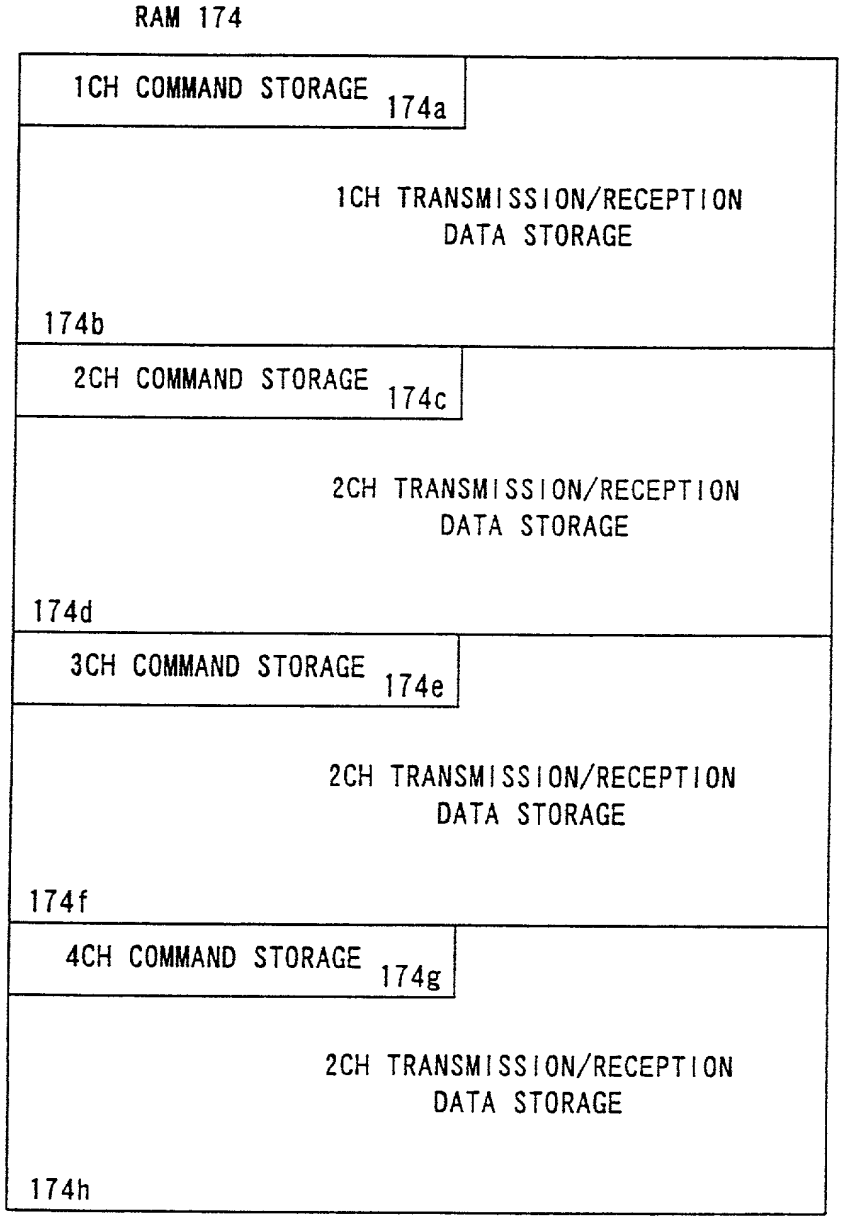

RAM 174
1CH COMMAND STORAGE 174a
1CH TRANSMISSION/RECEPTION DATA STORAGE
174b
2CH COMMAND STORAGE 174c
2CH TRANSMISSION/RECEPTION DATA STORAGE
174d
3CH COMMAND STORAGE 174e
2CH TRANSMISSION/RECEPTION DATA STORAGE
174f
4CH COMMAND STORAGE 174g
2CH TRANSMISSION/RECEPTION DATA STORAGE
174h

FIG. 7

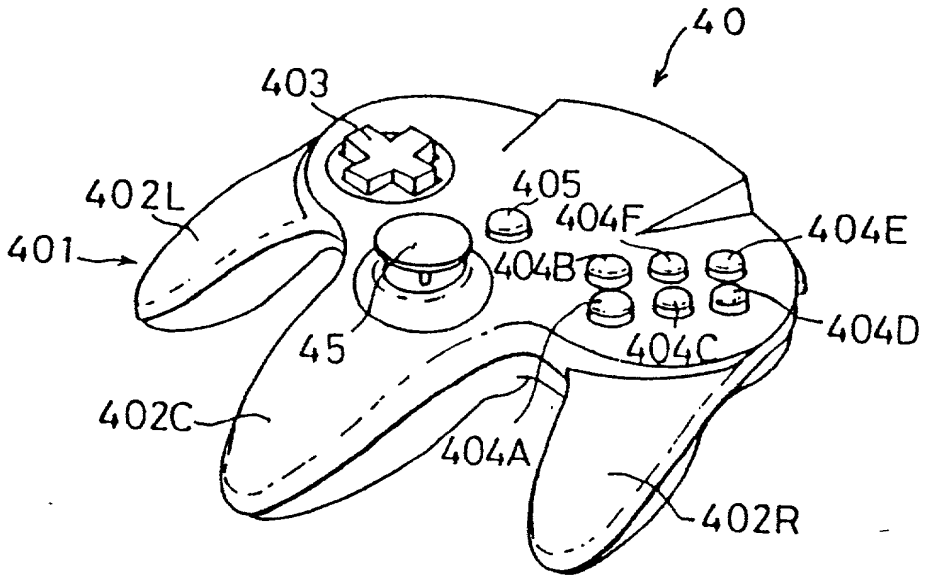

40
403
402L
401
405
404F
404E
404B
404D
45
404C
402C
404A
402R

FIG. 8

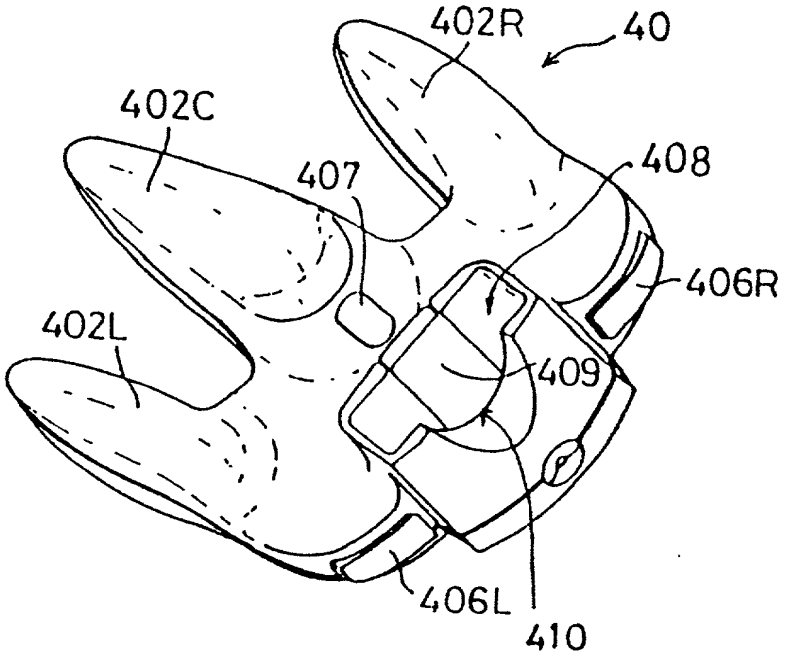

402R
40
402C
407
408
406R
402L
409
406L
410

FIG. 9

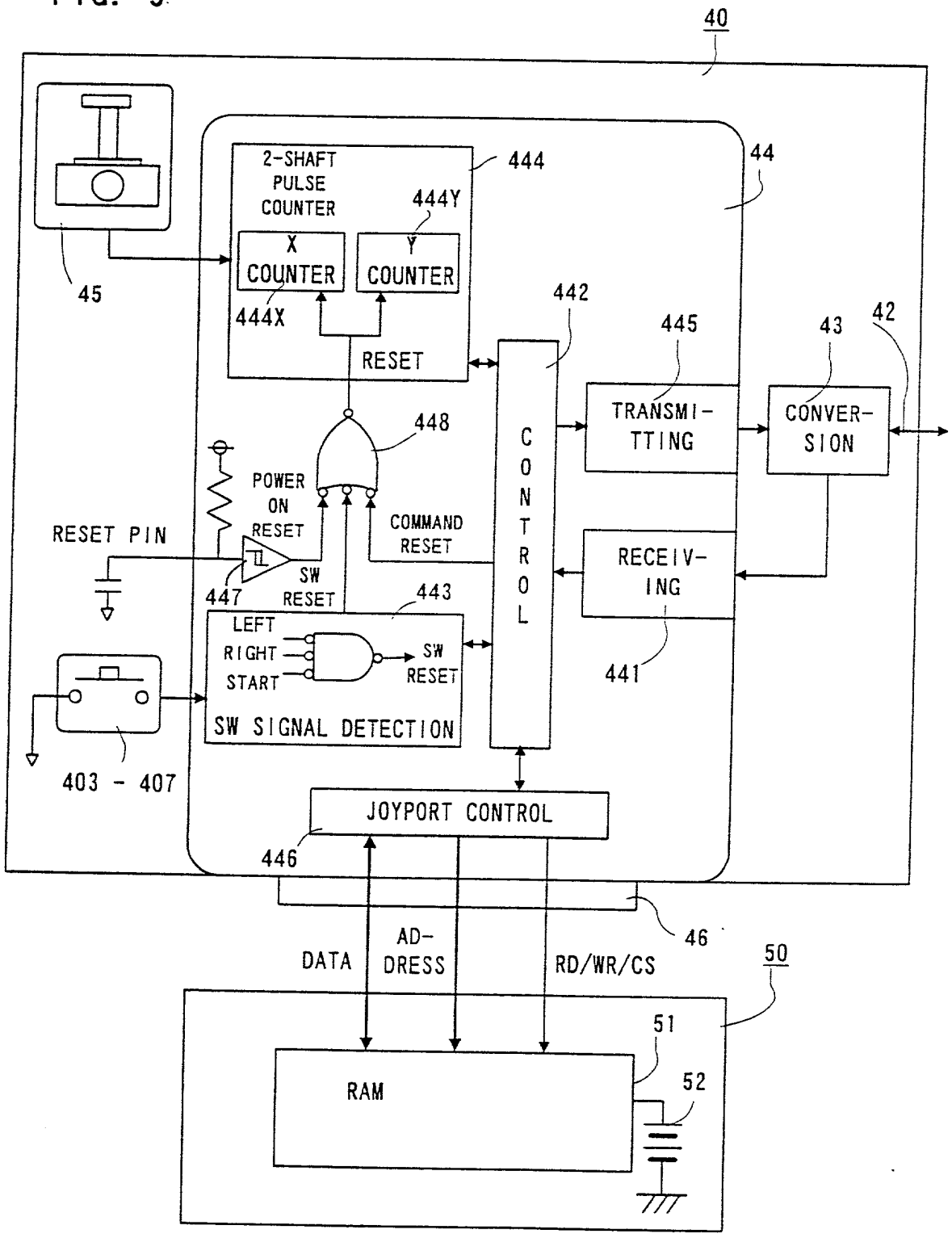

40
44
2-SHAFT PULSE COUNTER
444
444Y
X COUNTER
Y COUNTER
444X
45
RESET
442
445
43
42
448
POWER ON RESET
TRANSMI-TTING
CONVER-SION
CONTROL
RESET PIN
COMMAND RESET
RECEIV-ING
447
SW RESET
443
LEFT
RIGHT
START
SW RESET
441
SW SIGNAL DETECTION
403 - 407
JOYPORT CONTROL
446
46
DATA
AD-DRESS
RD/WR/CS
50
51
RAM
52

FIG. 10

1 BYTE	B	A	G	START	↑	↓	←	→
2 BYTE	JSRST	0	L	R	E	D	C	F
3 BYTE	X ORDINATE							
4 BYTE	Y ORDINATE							

FIG. 11

COMMAND 0: TRANSMITTING TYPE OF COMMAND
RECEPTION : 1 BYTE TRANSMISSION : 3 BYTES

		d7	d6	d5	d4	d3	d2	d1	d0
RECEPTION	1 BYTE	← COMMAND 0 →							
TRANSMISSION	1 BYTE	← TYPE L →							
	2 BYTE	← TYPE H →							
	3 BYTE	← STATUS →							

FIG. 12

COMMAND 1: ACCESSING STANDARD CONTROLLER
RECEPTION : 1 BYTE TRANSMISSION : 4 BYTES

		d7	d6	d5	d4	d3	d2	d1	d0
RECEPTION	1 BYTE	← COMMAND 1 →							
TRANSMISSION	1 BYTE	B	A	G	START	↑	↓	←	→
	2 BYTE	JSRST*	0	L	R	E	D	C	F
	3 BYTE	← X ORDINATE →							
	4 BYTE	← Y ORDINATE →							

* HIGH LEVEL AT TIME THAT L, R, START BUTTONS ARE SIMULTANEOUSLY DEPRESSED

FIG. 13

COMMAND 2: READ-OUT RAM
RECEPTION: 3 BYTES TRANSMISSION: 33 BYTES

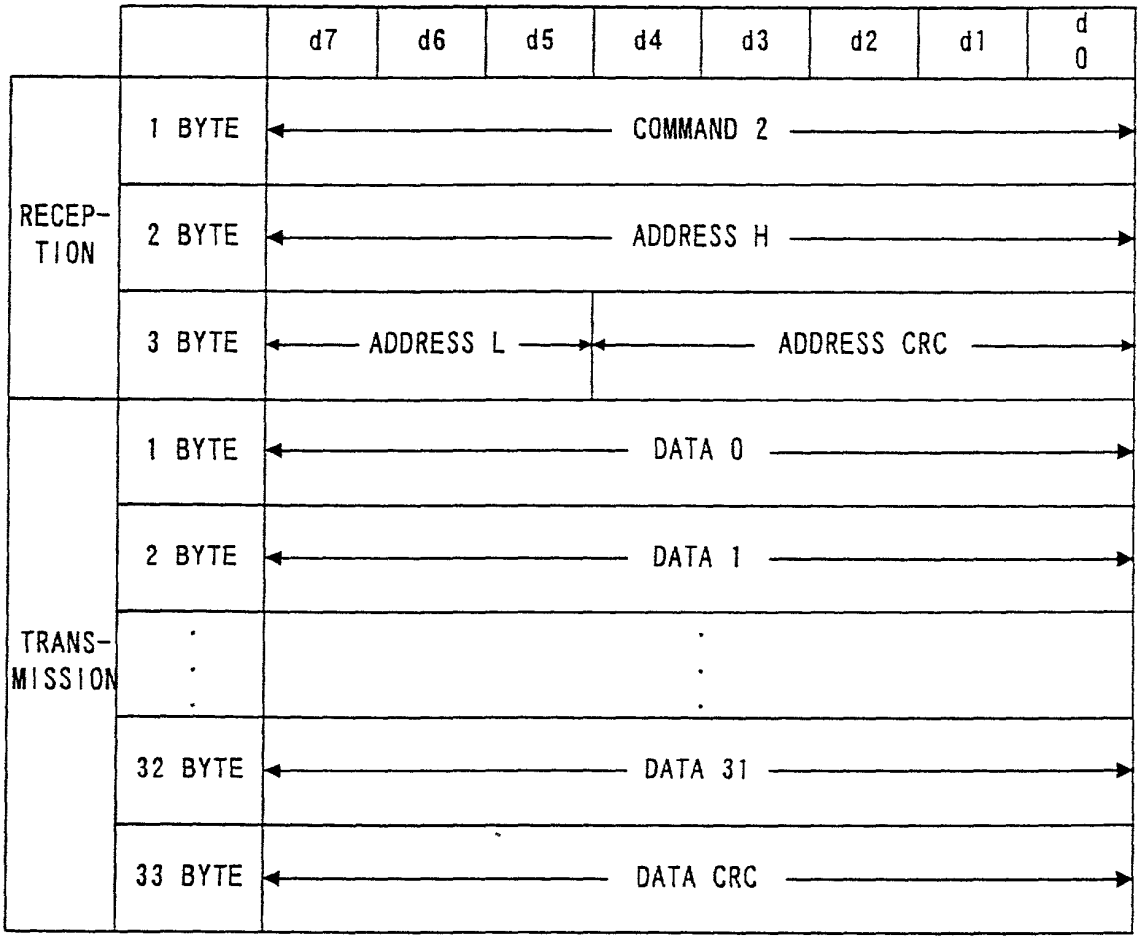


FIG. 14

COMMAND 3: WRITING INTO RAM
RECEPTION: 35 BYTES TRANSMISSION: 1 BYTE

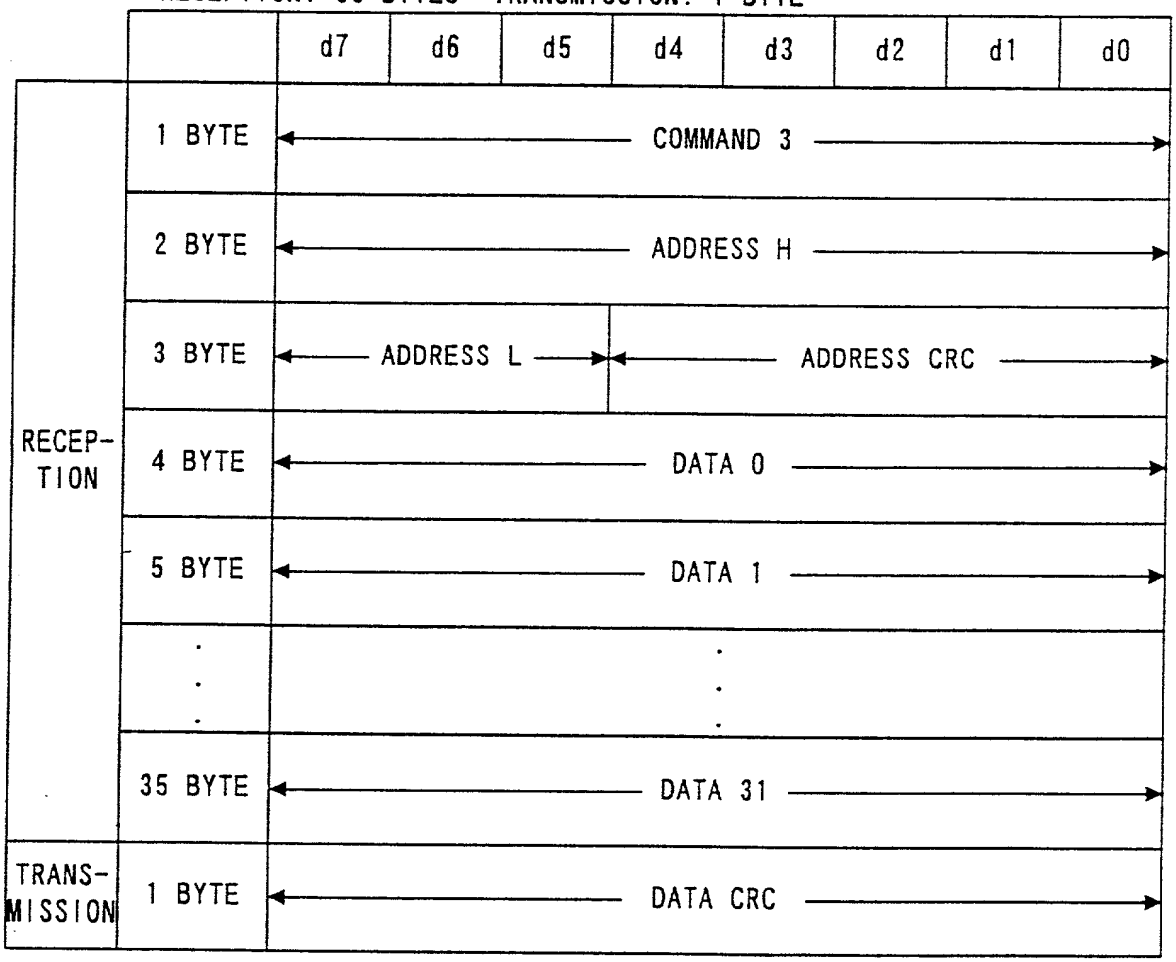


FIG. 15

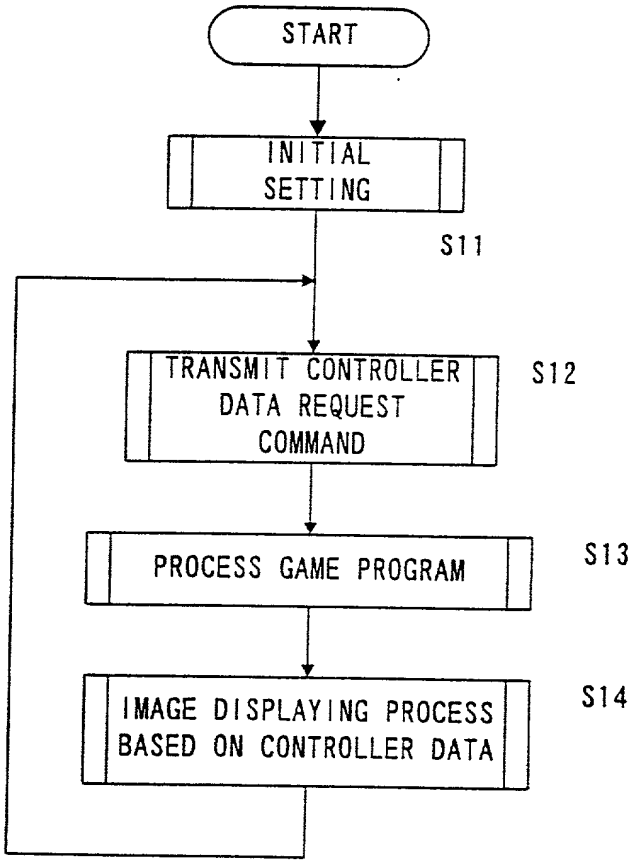

START
INITIAL SETTING
S11
TRANSMIT CONTROLLER DATA REQUEST COMMAND
S12
PROCESS GAME PROGRAM
S13
IMAGE DISPLAYING PROCESS BASED ON CONTROLLER DATA
S14

FIG. 16

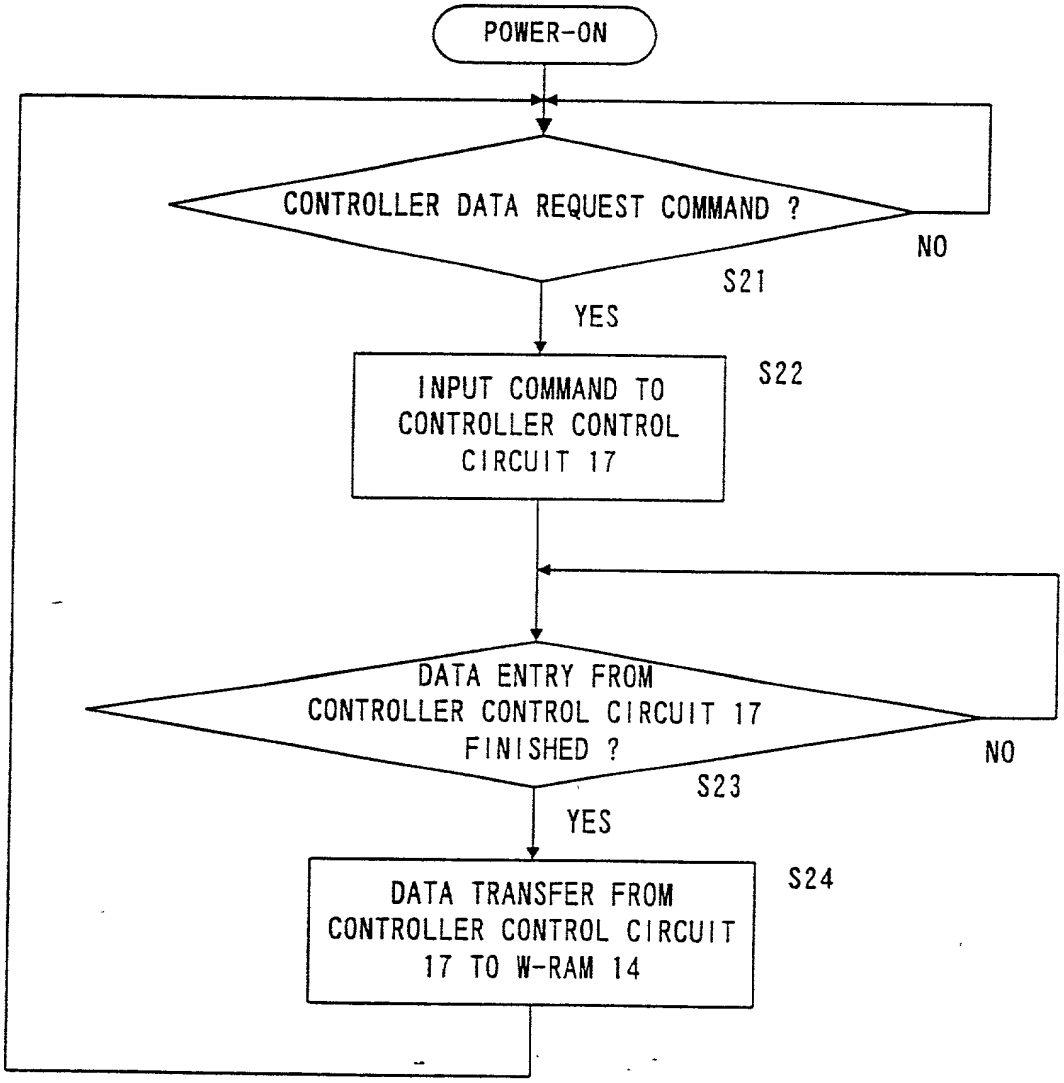

POWER-ON
CONTROLLER DATA REQUEST COMMAND ?
NO
S21
YES
INPUT COMMAND TO CONTROLLER CONTROL CIRCUIT 17
S22
DATA ENTRY FROM CONTROLLER CONTROL CIRCUIT 17 FINISHED ?
NO
S23
YES
DATA TRANSFER FROM CONTROLLER CONTROL CIRCUIT 17 TO W-RAM 14
S24

FIG. 17

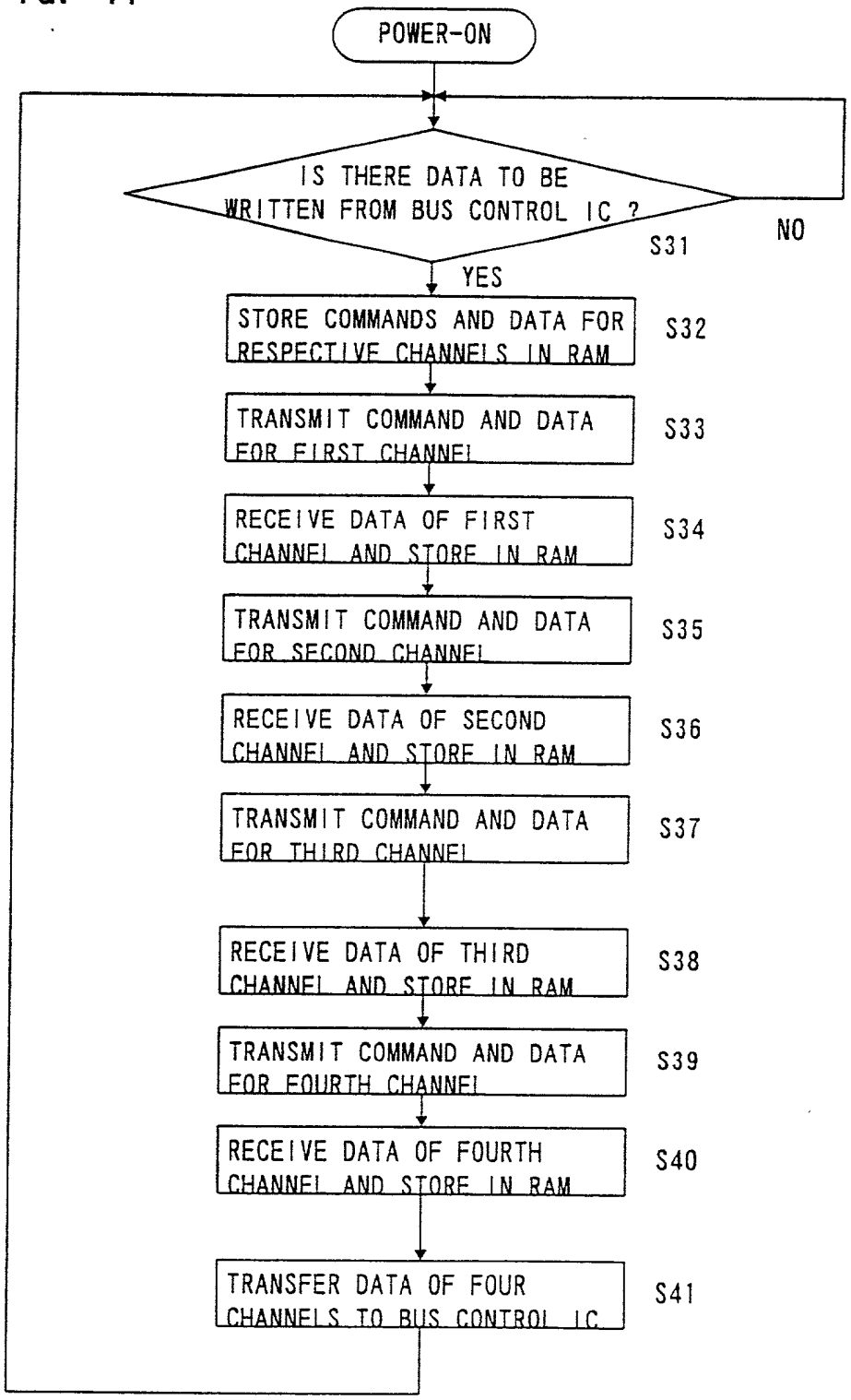

POWER-ON
IS THERE DATA TO BE WRITTEN FROM BUS CONTROL IC ?
S31
NO
YES
STORE COMMANDS AND DATA FOR RESPECTIVE CHANNELS IN RAM
S32
TRANSMIT COMMAND AND DATA FOR FIRST CHANNEL
S33
RECEIVE DATA OF FIRST CHANNEL AND STORE IN RAM
S34
TRANSMIT COMMAND AND DATA FOR SECOND CHANNEL
S35
RECEIVE DATA OF SECOND CHANNEL AND STORE IN RAM
S36
TRANSMIT COMMAND AND DATA FOR THIRD CHANNEL
S37
RECEIVE DATA OF THIRD CHANNEL AND STORE IN RAM
S38
TRANSMIT COMMAND AND DATA FOR FOURTH CHANNEL
S39
RECEIVE DATA OF FOURTH CHANNEL AND STORE IN RAM
S40
TRANSFER DATA OF FOUR CHANNELS TO BUS CONTROL IC
S41

FIG. 18

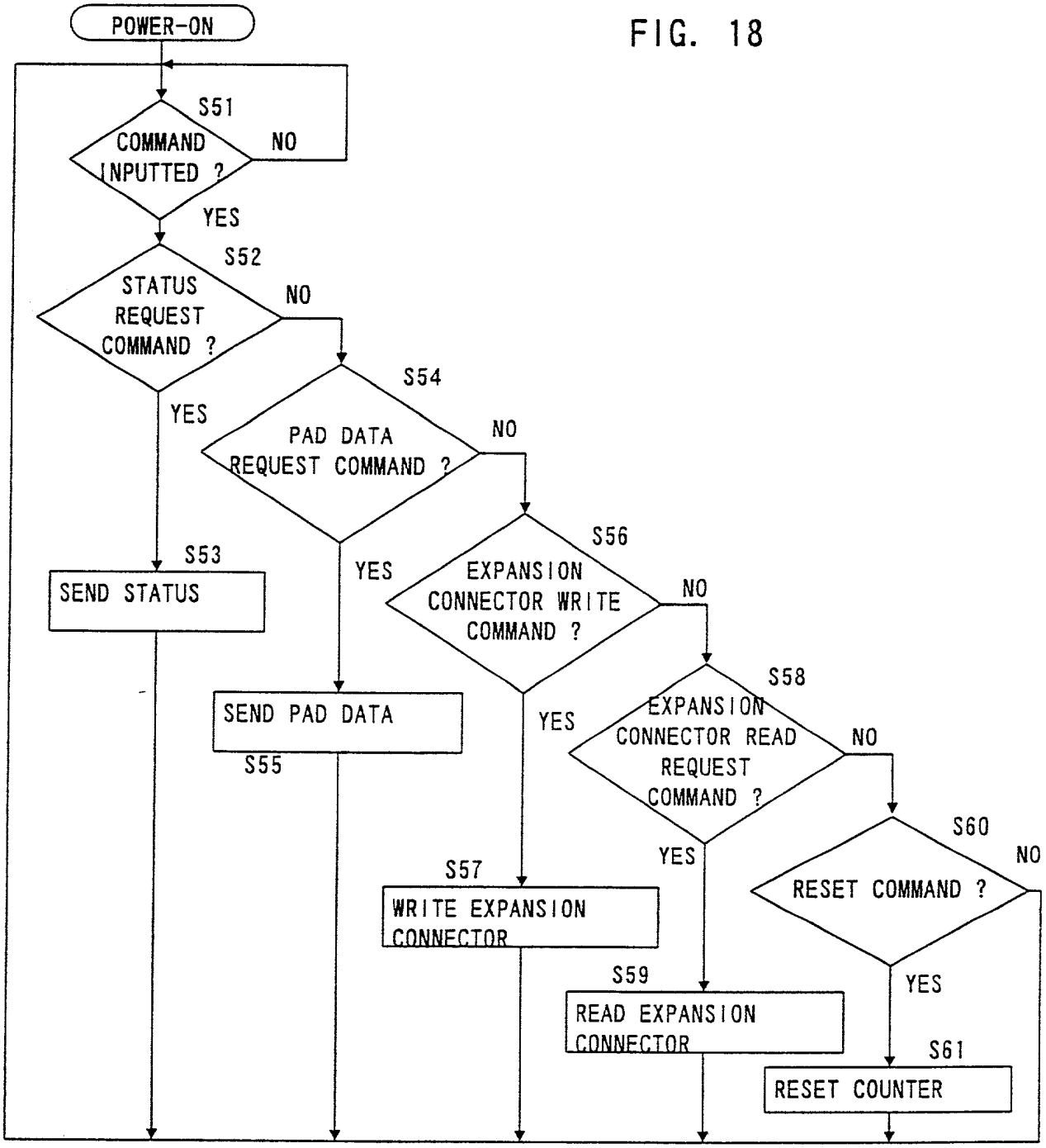

POWER-ON
S51
COMMAND INPUTTED ?
NO
YES
S52
STATUS REQUEST COMMAND ?
NO
YES
S54
PAD DATA REQUEST COMMAND ?
NO
YES
S56
EXPANSION CONNECTOR WRITE COMMAND ?
NO
YES
S58
EXPANSION CONNECTOR READ REQUEST COMMAND ?
NO
YES
S60
RESET COMMAND ?
NO
YES
S53
SEND STATUS
S55
SEND PAD DATA
S57
WRITE EXPANSION CONNECTOR
S59
READ EXPANSION CONNECTOR
S61
RESET COUNTER

FIG. 19

COMMAND 255: CONTROLLER RESET
RECEPTION: 1 BYTE TRANSMISSION: 3 BYTES

		d7	d6	d5	d4	d3	d2	d1	d0
RECEPTION	1 BYTE	← COMMAND 255 →							
TRANSMISSION	1 BYTE	← TYPE L →							
	2 BYTE	← TYPE H →							
	3 BYTE	← STATUS →							

FIG. 20

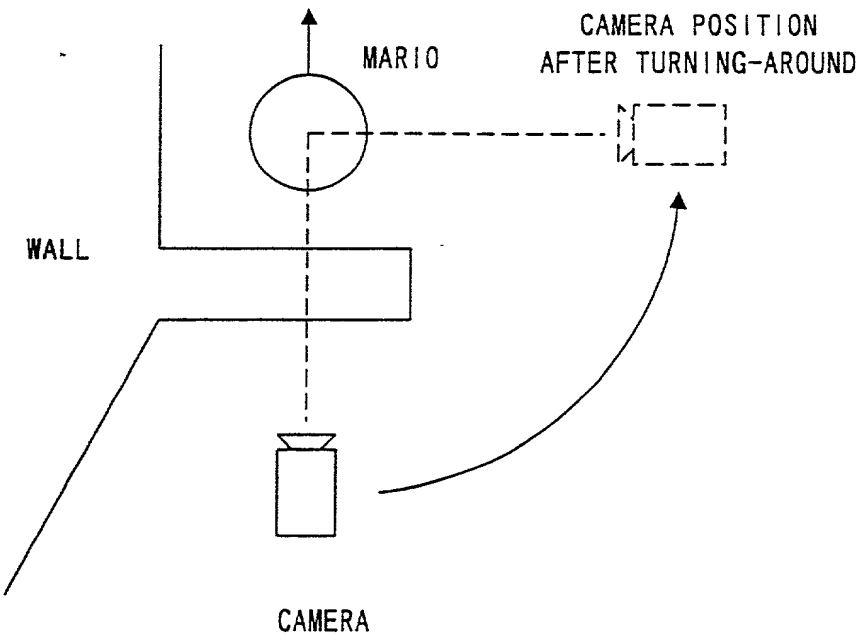


FIG. 21

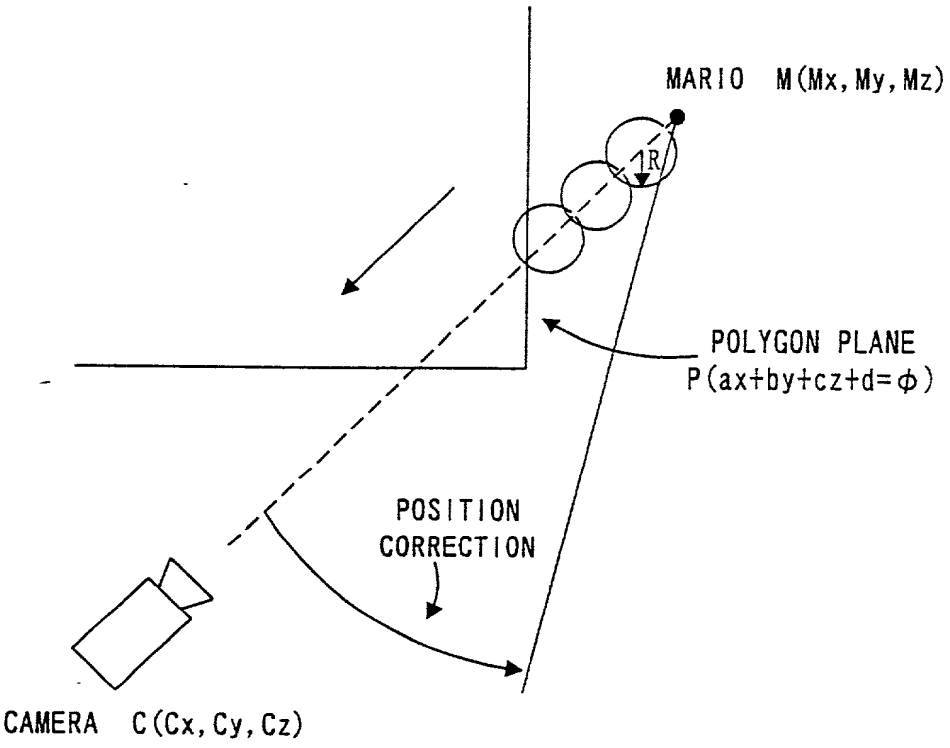

MARIO M(Mx, My, Mz)
R
POLYGON PLANE
P(ax+by+cz+d=φ)
POSITION
CORRECTION
CAMERA C(Cx, Cy, Cz)

FIG. 22

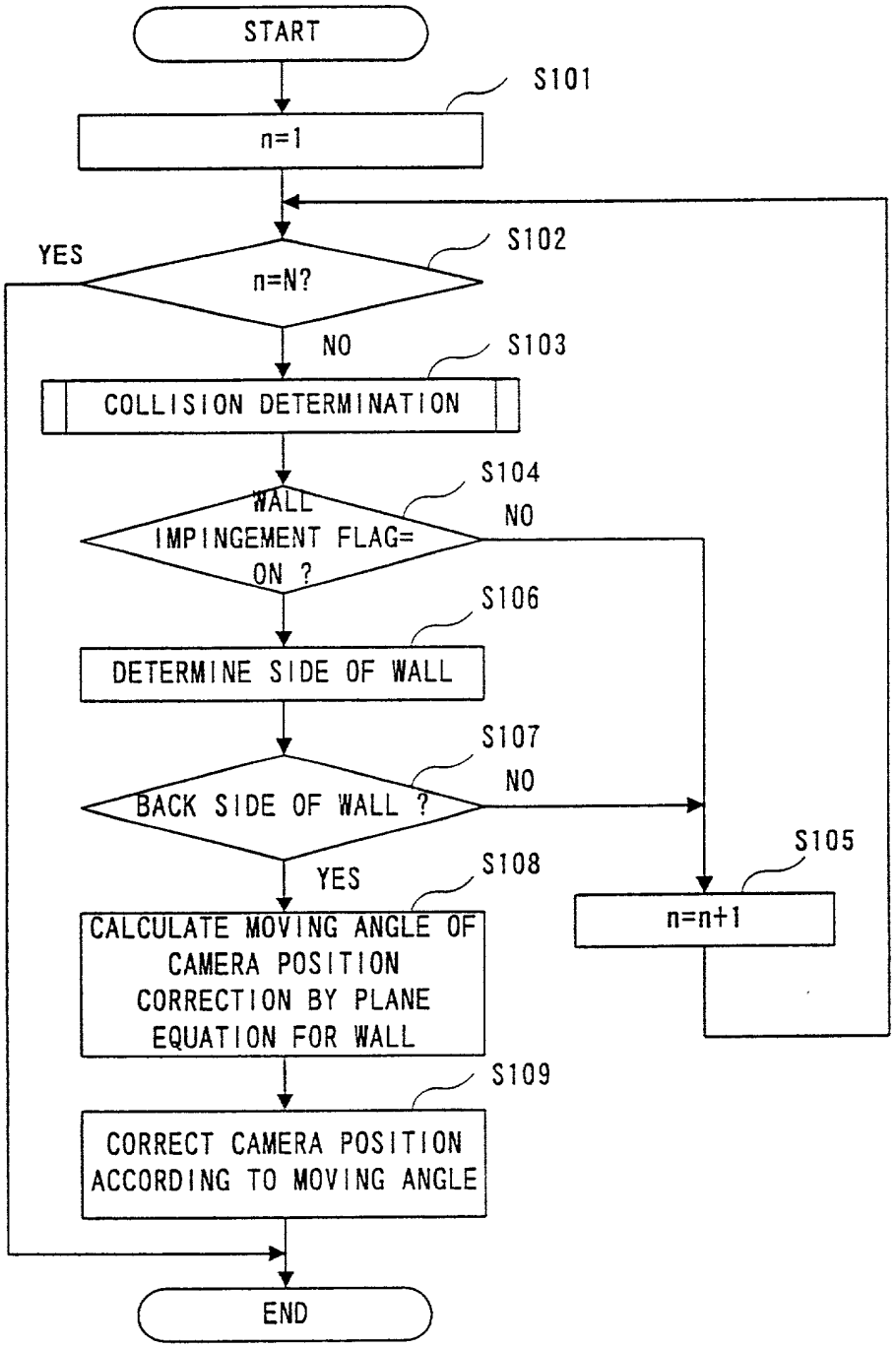

START
S101
n=1
S102
YES
n=N?
NO
S103
COLLISION DETERMINATION
S104
WALL IMPINGEMENT FLAG= ON ?
NO
S106
DETERMINE SIDE OF WALL
S107
BACK SIDE OF WALL ?
NO
S105
n=n+1
YES
S108
CALCULATE MOVING ANGLE OF CAMERA POSITION CORRECTION BY PLANE EQUATION FOR WALL
S109
CORRECT CAMERA POSITION ACCORDING TO MOVING ANGLE
END

FIG. 23

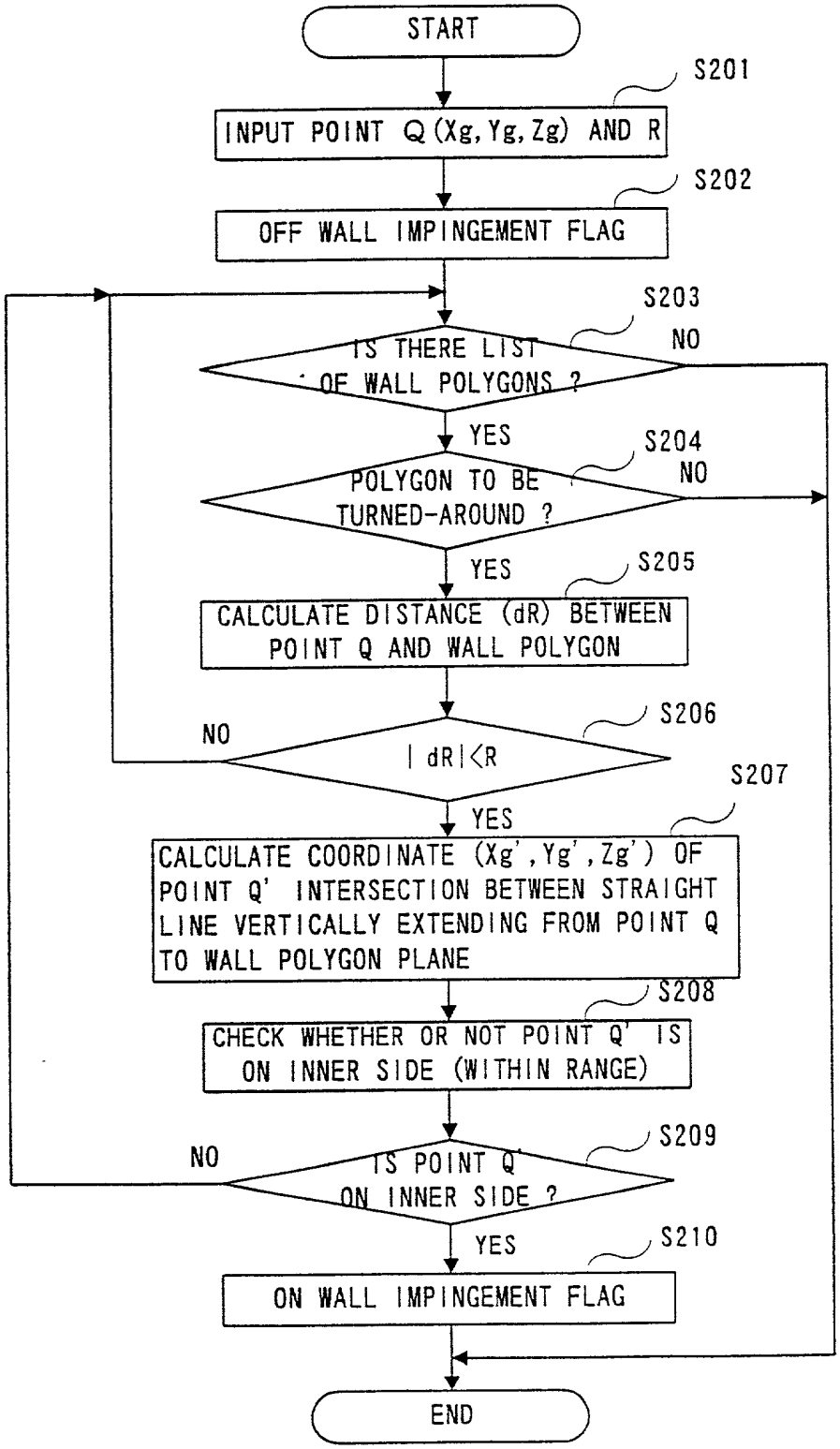

START
S201
INPUT POINT Q(Xg, Yg, Zg) AND R
S202
OFF WALL IMPINGEMENT FLAG
S203
IS THERE LIST OF WALL POLYGONS ?
NO
YES
S204
POLYGON TO BE TURNED-AROUND ?
NO
YES
S205
CALCULATE DISTANCE (dR) BETWEEN POINT Q AND WALL POLYGON
S206
NO
|dR|<R
S207
YES
CALCULATE COORDINATE (Xg', Yg', Zg') OF POINT Q' INTERSECTION BETWEEN STRAIGHT LINE VERTICALLY EXTENDING FROM POINT Q TO WALL POLYGON PLANE
S208
CHECK WHETHER OR NOT POINT Q' IS ON INNER SIDE (WITHIN RANGE)
S209
NO
IS POINT Q' ON INNER SIDE ?
YES
S210
ON WALL IMPINGEMENT FLAG
END

FIG. 24

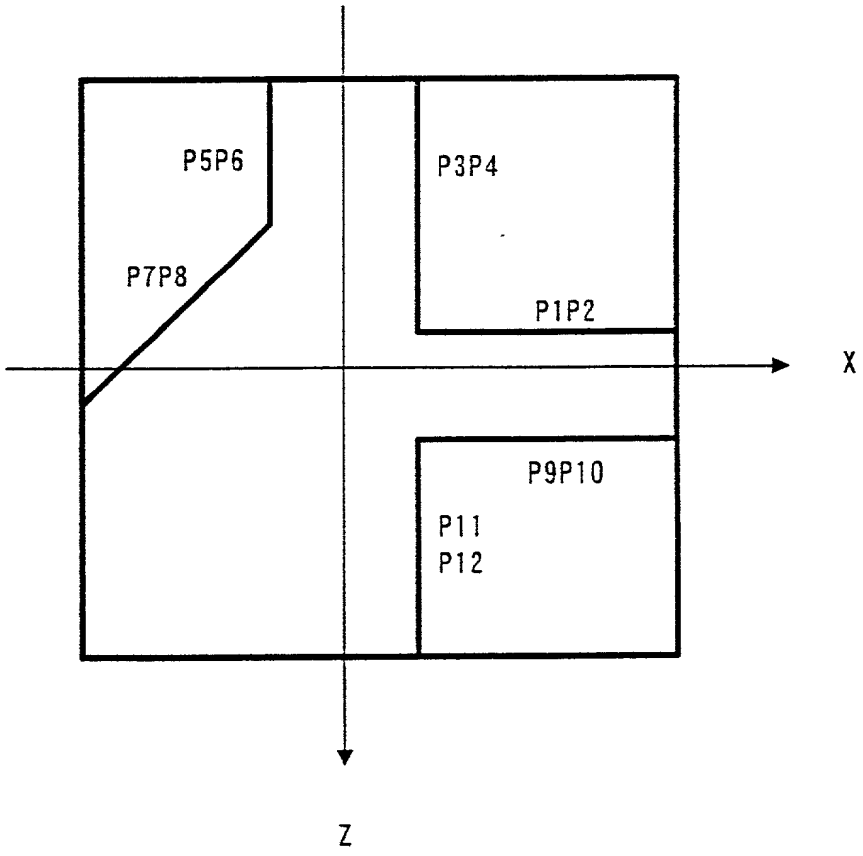


FIG. 25

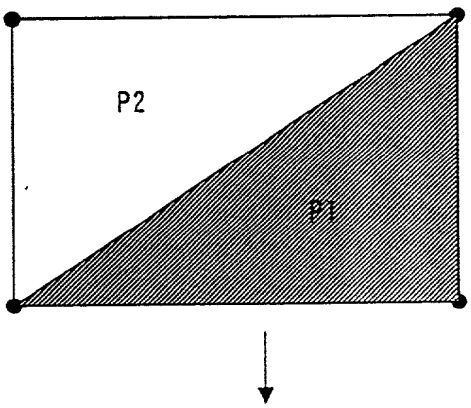


FIG. 26

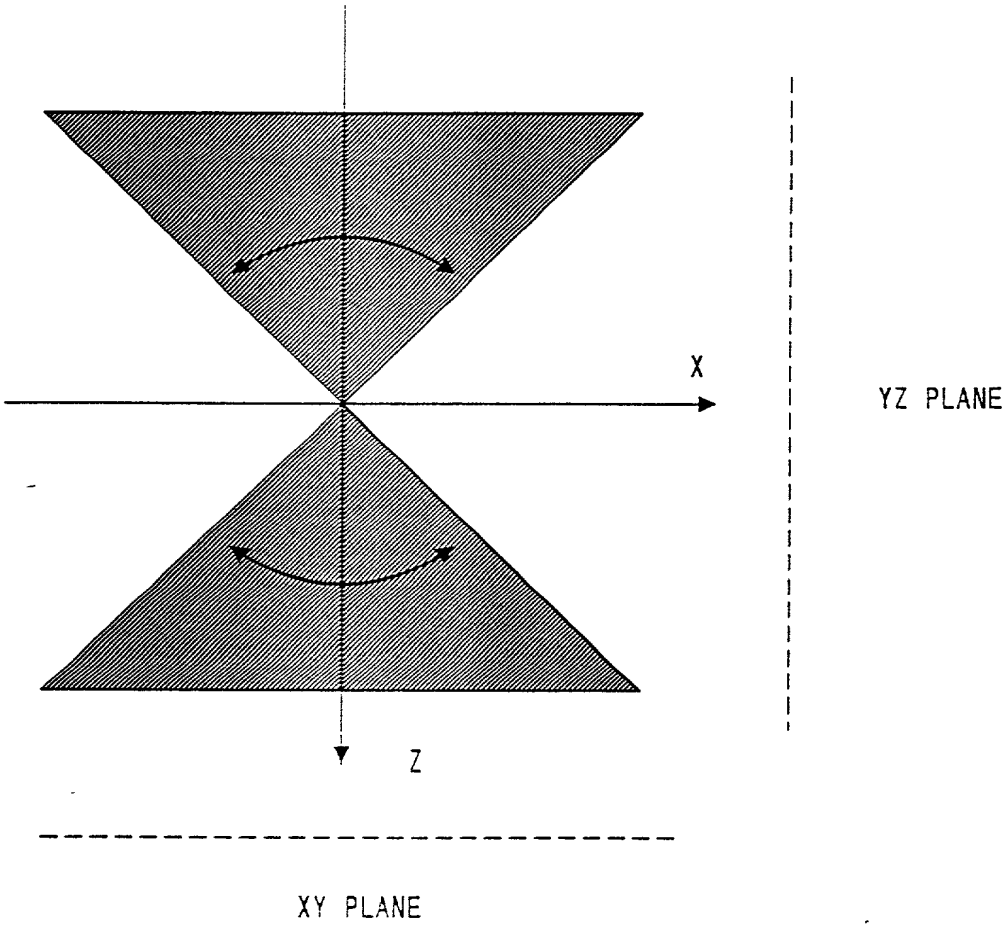


FIG. 27

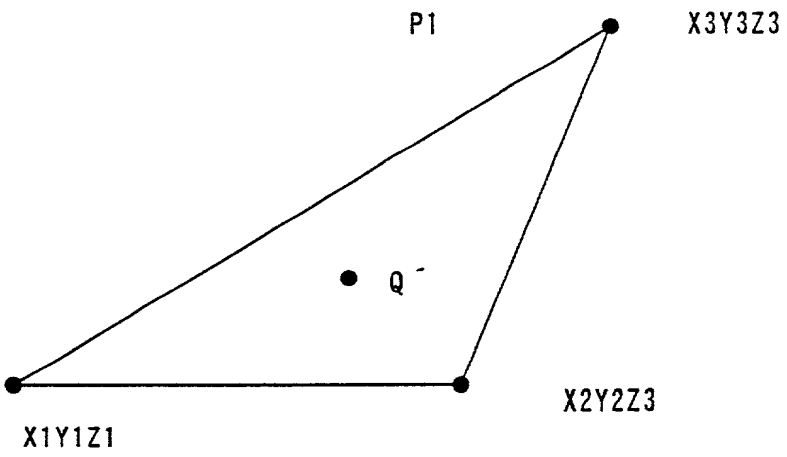


FIG. 28

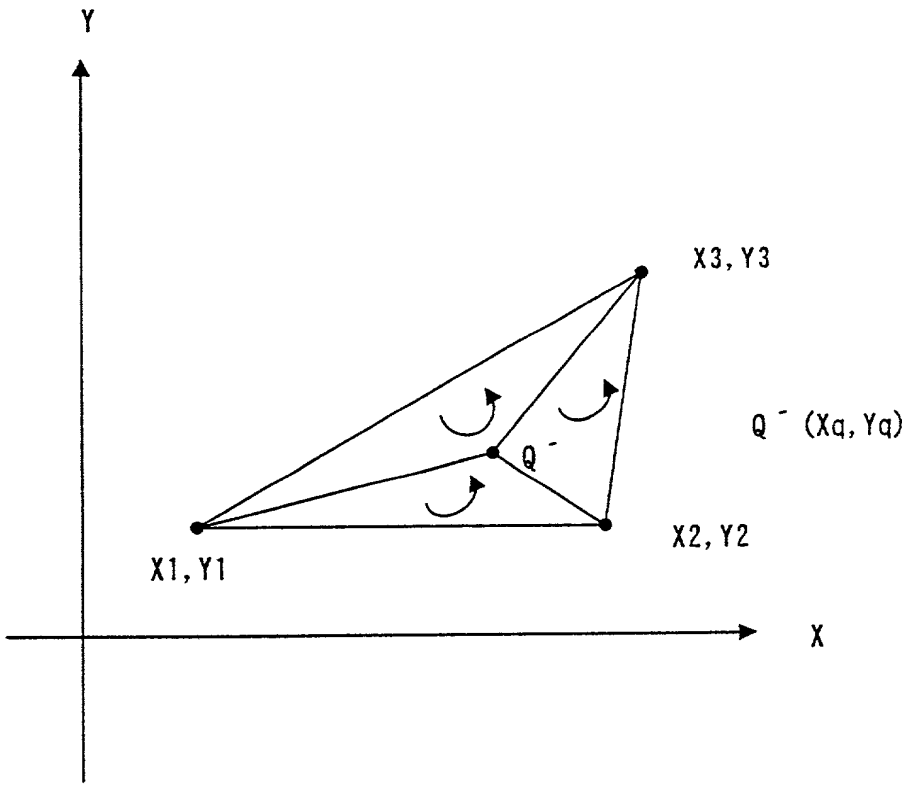
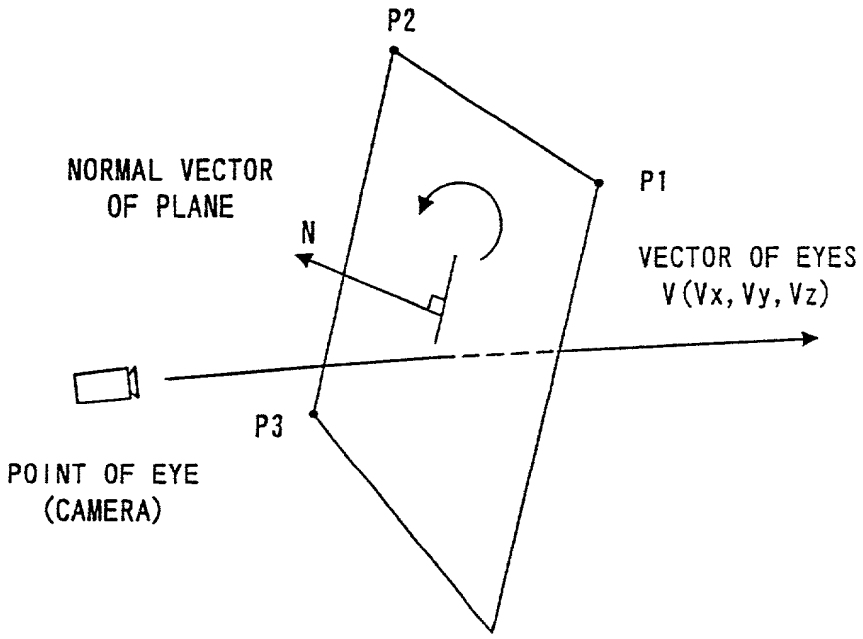


FIG. 29


P2
NORMAL VECTOR
OF PLANE
N
P1
VECTOR OF EYES
V(Vx, Vy, Vz)
P3
POINT OF EYE
(CAMERA)